DATA IMAGE CORPORATION

LCD Module Specification

ITEM NO.: **TG963220GRNNB-01**

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R&D Dept.	Q.C. Dept.	Eng. Dept.	Prod. Dept.
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2. RECORD OF REVISION

Rev	Date	Item	Page	Comment

3. GENERAL SPECIFICATIONS

Display Format :	96 (W)	×	32 (H)		Dots
Dot Size :	0.3 (W)	×	0.33 (H)		mm
Dot Pitch	0.31 (W)	×	0.34 (H)		mm
View Area :	35 (W)	×	13 (H)		mm
General Dimensions :	39 (W)	×	40.02 (H)	×	2.2 (T) mm Max.

Weight : 10 g max.

LCD Type : [V] STN Gray [ ] STN Yellow [ ] FSTN

Polarizer mode : [V] Reflective [ ] Transflective

[ ] Transmissive [ ] Negative

View Angle : [V] 6 O'clock [ ] 12 O'clock [ ] Others ____

Backlight : [ ] LED [ ] EL [ ] CCFL

Backlight Color : [ ] Yellow green [ ] Amber [ ] Blue Green

[ ] White [ ] Others

Controller / Driver : SED1530TAA

Temperature Range :

[ ] Normal		[V] Wide Temperature	
Operating	0 to 50°C	Operating	-20 to 70°C
Storage	-20 to 70°C	Storage	-30 to 80°C

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

V_{SS}= 0V, Ta = 25°C

Item	Symbol	Min.	Max.	Unit
Supply Voltage (Logic)	V_{DD}-V_{SS}	0	8	V
Supply Voltage (LCD Driver)	V_{DD}-V_{EE}	0	16.5	V
Input Voltage	V_I	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	-20	70	°C
Storage Temperature	T_{STG}	-30	80	°C

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Comment
	(Min.)	Max.)	(Min.)	(Max.)	
Ambient Temp	-20	70	-30	80	Note (1)
Humidity	Note (2)		Note(2)		Without Condensation
Vibration	--	4.9M/S^2	--	19.6M/S^2	XYZ Direction
Shock	--	29.4M/S^2	--	490M/S^2	XYZ Direction

Note(1) Ta = 0°C : 50Hr Max.
Note(2) Ta ≤ 40°C : 90% RH Max.
Ta ≥ 40°C : Absolute humidity must be lower than the humidity of 90% RH at 40°C.

5. ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (Logic)	V_{DD}-V_{SS}		2.7	3.3	5.5	V
Supply Voltage (LCD)	V_{DD}-V_{EE}	0°C	5.2	5.5	5.8	V
		25°C	4.7	5.0	5.3	
		50°C	4.2	4.5	4.8	
Input Voltage	V_{IH}	--	$V_{SS+2.0}$	--	V_{DD}	V
	V_{IL}		V_{SS}	--	$V_{SS+0.8}$	
Logic Supply Current	I_{DD}		--	0.7	--	mA

6. ELECTRO-OPTICAL CHARACTERISTICS

ITEM	Symbol	Condition	Min.	Typ.	Max.	Unit	Ref.
Rise Time	Tr	0°C		--	--	ms	Note (1)
		25°C		130	260		
Fall Time	Tf	0°C		--	--	ms	
		25°C		180	360		
Contrast	CR	25°C	2	5	--		Note (3)
View Angle	θ1~θ2 ∅1, ∅2	25°C & CR≥2	60	--	--	Degree	Note (2)
			90	--	--		
Frame Frequency	Ff	25°C	--	70	--	Hz	

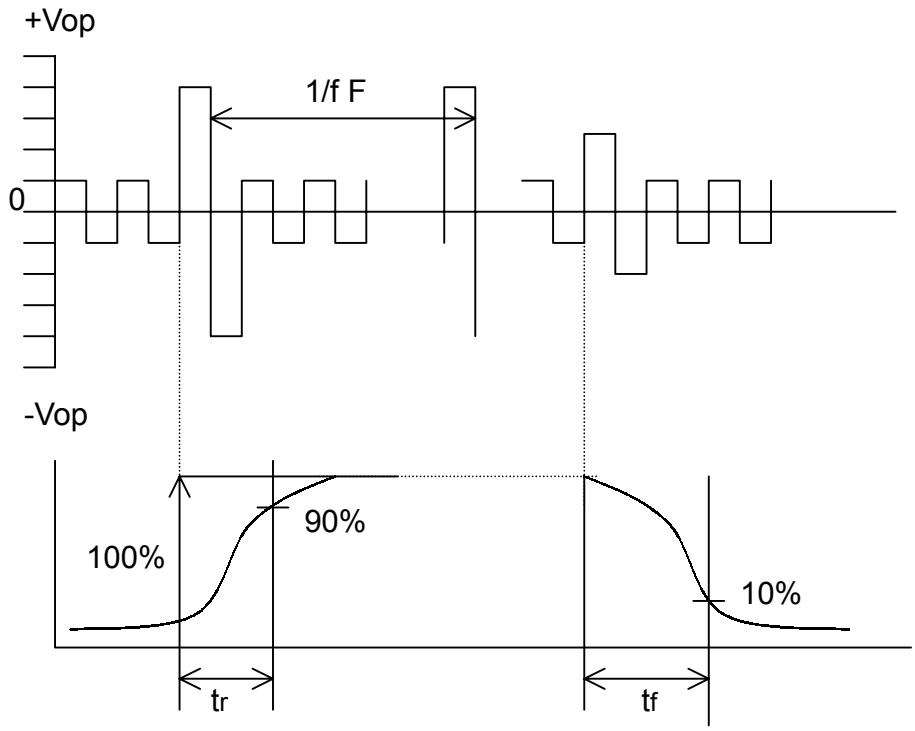
Note (1) & (2) : See next page

Note (3) : Contrast ratio is defined under the following condition:

$$CR = \frac{\text{Brightness of non-selected condition}}{\text{Brightness of selected condition}}$$

(a). Temperature ---------- 25°C
(b). Frame frequency ---- 70Hz
(c). Viewing angle -------- θ= 0°, ∅ = 0°
(d). Operating voltage --- 5.0V

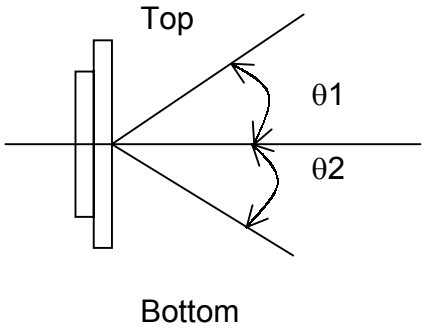
Note (1) Response time is measured as the shortest period of time possible between the change in state of an LCD segment as demonstrated below:



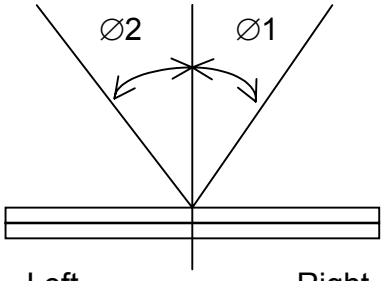
Condition:
(a) . Temperature ----------25°C
(b) . Frame frequency --------- 70Hz
(c) . View Angle ---------- θ = 0°, ∅=0°
(d) . Operating voltage -------- 5.0V

Note (2) Definition of View Angle

Top – Bottom direction



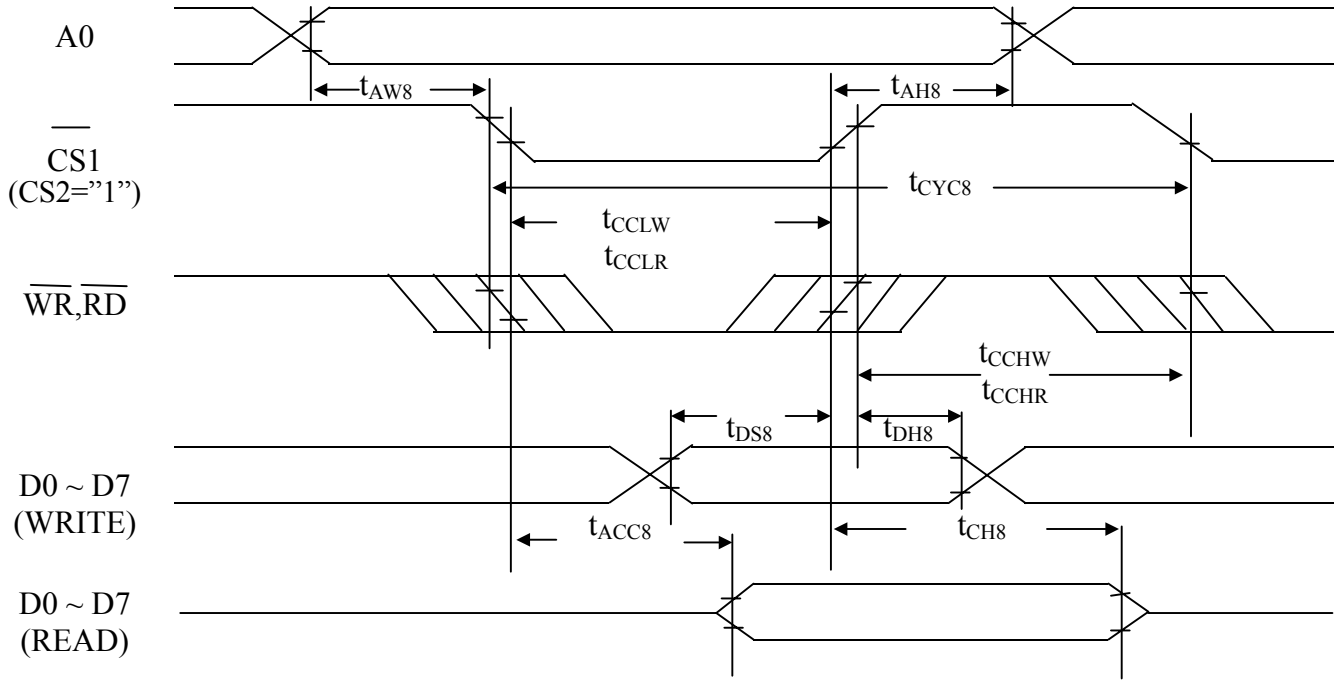
Right -- Left direction



7. TIMING CHARACTERISTICS

AC Characteristics

(1)System buses Read/write characteristics I (8080series microprocessor)



V_{DD}=5.0V±10%,Ta=-40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		10	--	ns
Address setup time		t_{AW8}		10	--	ns
System cycle time		t_{CYC8}		166	--	ns
Control L pulse width(WR)	$\overline{WR}$	t_{CCLW}		30	--	ns
Control L pulse width(RD)	$\overline{RD}$	t_{CCLR}		70	--	ns
Control H pulse width(WR)	$\overline{WR}$	t_{CCHW}		100	--	ns
Control H pulse width(RD)	$\overline{RD}$	t_{CCHR}		70	--	ns
Data setup time		t_{DS8}		20	--	ns
Data hold time		t_{DH8}		10	--	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	CL=100pF	--	70	ns
Output disable time		t_{CH8}		10	50	ns

V_{DD}=2.7V to 4.5V,Ta= - 40 to +85°C

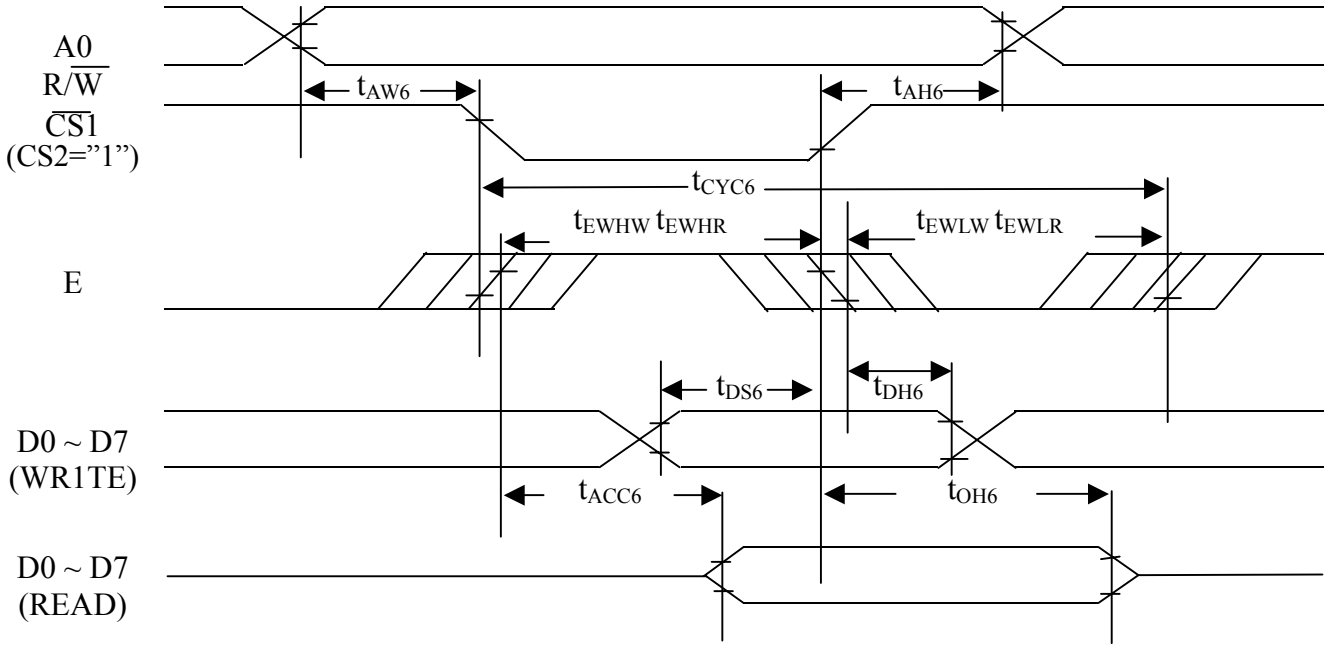
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		19	--	ns
Address setup time		t_{AW8}		15	--	ns
System cycle time		t_{CYC8}		450	--	ns
Control L pulse width(WR)	$\overline{WR}$	t_{CCLW}		60	--	ns
Control L pulse width(RD)	$\overline{RD}$	t_{CCLR}		140	--	ns
Control H pulse width(WR)	$\overline{WR}$	t_{CCHW}		200	--	ns
Control H pulse width(RD)	$\overline{RD}$	t_{CCHR}		140	--	ns
Data setup time		t_{DS8}		40	--	ns
Data hold time		t_{DH8}		15	--	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	CL=100pF	--	140	ns
Output disable time		t_{CH8}		10	100	ns

Notes:1.The input signal rise/fall time (t_r,t_f) is specified at 15 ns or less. When system cycle time is used at a high speed, it is specified by $t_r+t_f \leqq (t_{CYC8} - t_{CCLW})$ or $t_r+t_f \leqq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.

2.Every timing is specified on the basis of 20% and 80% of V_{DD} .

3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which $\overline{CS1}$ is "0"(CS="1") and $\overline{WR}$ and $\overline{RD}$ are"0".

(2)System buses Read/write characteristics II (6800-series microprocessor)



V_{DD}=5.0V±10%,Ta=-40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		166	--	ns
Address hold time		A0	t_{AH6}		10	--	ns
Address setup time		W/R	t_{AW6}		10	--	ns
Data setup time		D0 to D7	t_{DS6}		20	--	ns
Data hold time			t_{DH6}		10	--	ns
Output disable time			t_{OH6}	CL=100pF	10	50	ns
Access time			t_{ACC6}		--	70	ns
Enable Low pulse width	READ	E	t_{EWHR}		70	--	ns
	WRITE		t_{EWHW}		30	--	ns
Enable High pulse width	READ	E	t_{EWLR}		70	--	ns
	WRITE		t_{EWLW}		100	--	ns

V_{DD}=2.7V to 4.5V,Ta=-40 to +85°C

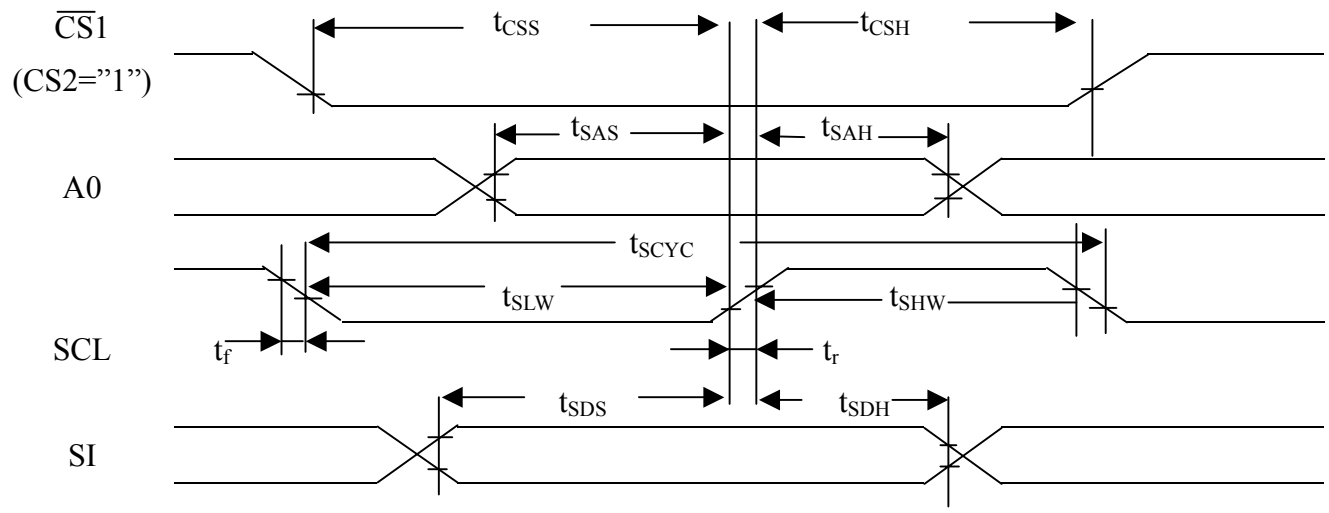
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		450	--	ns
Address hold time		A0	t_{AW6}		15	--	ns
Address setup time		R/ W	t_{AH6}		19	--	ns
Data setup time		D0 to D7	t_{DS6}		40	--	ns
Data hold time			t_{DH6}		15	--	ns
Output disable time			t_{OH6}	CL=100pF	10	100	ns
Access time			t_{ACC6}		--	140	ns
Enable Low pulse width	READ	E	t_{EWHR}		140	--	ns
	WRITE		t_{EWHW}		60	--	ns
Enable High pulse width	READ	E	t_{EWLR}		140	--	ns
	WRITE		t_{EWLW}		200	--	ns

Notes:1.The input signal rise/fall time (t_r,t_f) is specified at 15 ns or less. When system cycle time is used at a high speed, it is specified by $t_r+t_f \leqq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $t_r+t_f \leqq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.

2.Every timing is specified on the basis of 20% and 80% of V_{DD} .

3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which CS1 is "0"(CS2="1") and E is "1".

(3)System buses



V_{DD}=5.0V±10%,Ta=-40 to +85°C

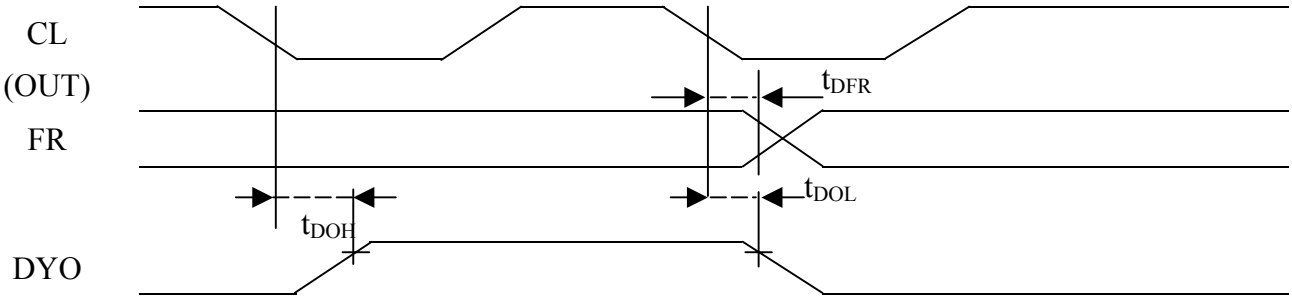
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}		250	--	ns
System clock H pulse width		t_{SHW}		100	--	ns
System clock L pulse width		t_{SLW}		75	--	ns
Address setup time	A0	t_{SAS}		50	--	ns
Address hold time		t_{SAH}		200	--	ns
Data setup time	SI	t_{SDS}		50	--	ns
Data hold time		t_{SDH}		50	--	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		30	--	ns
		t_{CSH}		100	--	

V_{DD}=2.7V to 4.5V,Ta=-40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}		500	--	ns
System clock H pulse width		t_{SHW}		200	--	ns
System clock L pulse width		t_{SLW}		150	--	ns
Address setup time	A0	t_{SAS}		100	--	ns
Address hold time		t_{SAH}		400	--	ns
Data setup time	SI	t_{SDS}		100	--	ns
Data hold time		t_{SDH}		100	--	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		60	--	ns
		t_{CSH}		200	--	

Notes:1.The input signal rise and fall times must be within 15 nanoseconds.
2.All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(4) **Display control timing**



Output timing V_{DD}=5.0V ±10%,Ta=-40 to +85°C

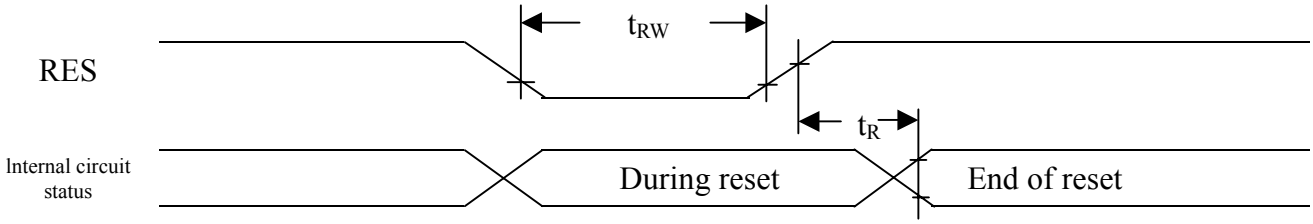
Parameter	Signal	Symbol	Condition	Min.	Typ	Max.	Unit
FR delay time	FR	t_{DFR}	C_L=50pF	--	10	40	ns
DYO "H" delay time	DYO	t_{DOH}		--	40	100	ns
DYO "L" delay time		t_{DOL}		--	40	100	ns

Output timing V_{SS}=0V, V_{DD}=2.7V 4.5V,Ta=to 40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ	Max.	Unit
FR delay time	FR	t_{DFR}	C_L=50pF	--	15	80	ns
DYO "H" delay time	DYO	t_{DOH}		--	70	200	ns
DYO "L" delay time		t_{DOL}		--	70	200	ns

Notes:1.The output timing is valid in master mode.
2.Every timing is specified on the basis of 20% and 80% of V_{DD}.

(5) Reset timing



V_{DD}=5.0V ±10%,Ta=-40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ	Max.	Unit
Reset time		t_R		0.5	--	--	μs
Reset low pulse width	$\overline{RES}$	t_{RW}		0.5	--	--	μs

V_{DD}=2.7V to 4.5V,Ta=-40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ	Max.	Unit
Reset time		t_R		1.0	--	--	μs
Reset low pulse width	$\overline{RES}$	t_{RW}		1.0	--	--	μs

Notes:1.The reset timing is specified on the basis of 20% and 80% of V_{DD}.

7.1. PIN DESCRIPTON

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5V power supply. Connect to microprocessor power supply pin V_{CC}.	2
V_{SS}	Supply	Ground	1
V_1,V_2 V_3,V_4 V_5	Supply	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When the 0n-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command. SED 1530 V1: 1/5 • V5 1/6 • V5 V2: 2/5 • V5 2/6 • V5 V3: 3/5 • V5 4/6 • V5 V4: 4/5 • V5 5/6 • V5	6

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1-	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2-	O	DC/DC voltage converter capacitor 2 negative connection	1
CAP3-	O	DC/DC voltage converter capacitor 1 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
VR	I	Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit microprocessor data bus. When the serial interface selects; D7:Serial data input(SI) D6:Serial clock input (SCL)	8
A0	I	Control/display data flag input. It is connected to the LSB of micro-processor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data.	1
$\overline{RES}$		When $\overline{RES}$ is caused to go low, initialization is executed. A reset operation is performed at the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when-CS1 is low and CS2 is high. When chip select is non-active, D0 to D7 will be “HZ”.	2
RD (E)	I	• When interfacing to an 8080 series microprocessor: Active low. This input connects the RD signal of the 8080 series microprocessor . While this signal is low, the SED1530 series data bus output is enabled. • When interfacing to a 6800 series microprocessor: Active high. This is used as an enable clock input pin of the 6800 series microprocessor.	1
$\overline{WR}$ (R/W)	I	• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active low. • When interfacing to an 6800-series microprocessor, it will be read mode when R/W is high and it will be write mode when R/$\overline{W}$ is low. R/$\overline{W}$= “1” :Read R/$\overline{W}$= “0” :Write	1

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>C86</td><td>I</td><td>Microprocessor interface select terminal.
C86=high: 6800 series microprocessor interface
C86=low: 8080 series microprocessor interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input select pin.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data/command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>“H”</td><td>$\overline{CS1}$,CS2</td><td>A0</td><td>D0-D7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>--</td></tr>
<tr><td>“L”</td><td>$\overline{CS1}$,CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL(D6)</td></tr>
</table>
*In serial mode, no data can be read from RAM.
When P/S= low, D0 to D5 are HZ and $\overline{RD}$ and $\overline{WR}$ must be fixed high or low</td><td>1</td></tr>
</table>

7.2. LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>M/S</td><td>I</td><td>SED1530 series master/slave mode select input. When a necessary signal is output to the LCD, the master operation is synchronized with the LCD system, while when a necessary signal is input to the LCD, the slave operation is synchronized with the LCD system.
M/S= high : Master operation
M/S= low : Slave operation
The following is provided depending on the M/S status.
<table>
<tr><th>Model</th><th>Status</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>DYO</th><th>FRS</th><th>DOF</th></tr>
<tr><td rowspan="2">SED153*D**</td><td>Master</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>Slave</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>HZ</td><td>HZ</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display Clock input/output. When the SED1530 series selects Master/ slave mode, each CL pin is connected. When it is used in combination with the common driver, this input/output is connected to common driver YSCL pin.
M/S= high: Output
M/S= low: input</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output. When the SED1530 series selects master/ slave mode, each FR pin is connected.
When the SED1530 series selects master mode this input/output is connected to the common driver FR pin.
M/S= high: Output
M/S= low: input</td><td>1</td></tr>
<tr><td>DYO</td><td>I/O</td><td>Common drive signal output. This output is enabled for only at master operation and connects to the common driver DIO pin. It becomes HZ at slave operation.</td><td>1</td></tr>
<tr><td>VS1</td><td>O</td><td>Internal power supply voltage monitor output.</td><td>1</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>LCD blanking control input/output. When the SED1530 series selects master/slave mode, the respective $\overline{DOF}$ pin is connected. When it is used in combination with the common driver (SED1635), this output/ input is connected to the common driver $\overline{DOFF}$ pin.
M/S= high: Output
M/S= low: input</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>Static drive output.
This is enabled only at master operation and used together with the FR pin. This output becomes HZ at slave operation.</td><td>1</td></tr>
</table>

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>On
(SEG n)
(Com n)</td><td>O</td><td>LCD drive output. The following assignment is made depending on the model.

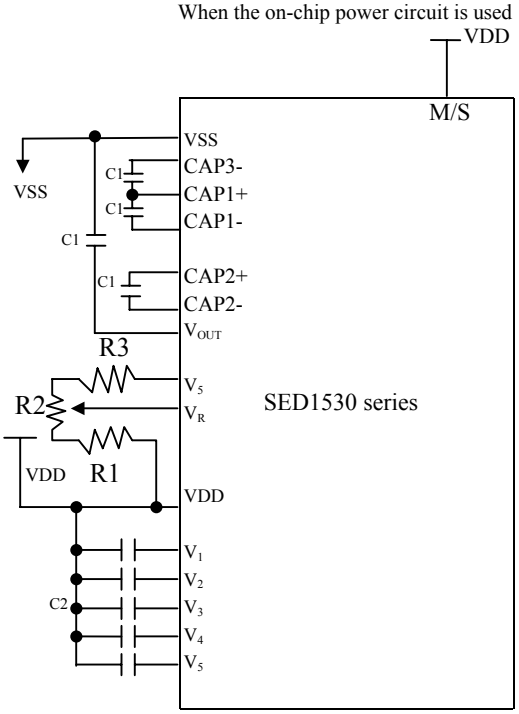
<table>
<tr><td></td><td>SEG</td><td>COM</td></tr>
<tr><td>SED 1530D0*</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>SED 1530DA*
SED 1530DF*</td><td>O16~O115</td><td>O0~O15,O116~O131</td></tr>
</table>
SEG output. LCD segment drive output. One of V_{DD},V_2,V_3 and V_5 levels is selected by combination of the contents of display RAM and FR signal.

<table>
<tr><td rowspan="2">RAM data</td><td rowspan="2">FR</td><td colspan="2">On output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">0</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>--</td><td colspan="2">V_{DD}</td></tr>
</table>
COM output. LCD common drive output. One of V_{DD},V_1,V_4 and V_5 levels is selected by combination of scan data and FR signal.

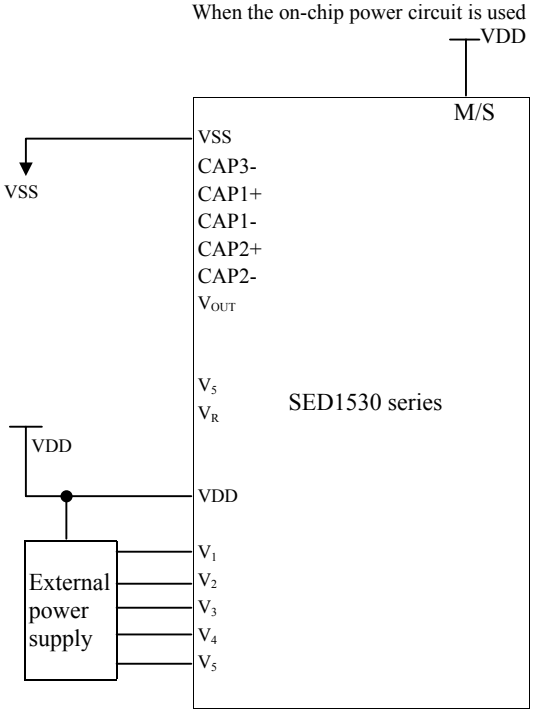
<table>
<tr><td>Scan data</td><td>FR</td><td>On output voltage</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td>--</td><td>V_{DD}</td></tr>
</table>
</td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. When it is not used, it is made open.
Effective only with the SED1530,SED1532,SED1533 and SED1534 and “HZ” with the SED1531.
When multiple numbers of the SED1530,SED1532,SED1533 and SED1534 are used, the same COMS signal is output to both master and slave units.</td><td></td></tr>
<tr><td></td><td></td><td>Total</td><td>172</td></tr>
</table>

7.3. VOLTAGE GENERATOR CIRCUIT

When the on-chip power circuit is used



When the on-chip power circuit is used



Reference setup value: SED1530 V_5 ≒ -7 to -9V
SED1531 V_5 ≒ -11 to -13V (variable)
SED1532 V_5 ≒ -11 to -13V (variable)

	SED1530	SED1531	SED1532
C1	1.0~4.7ufΩ	1.0~4.7uF	1.0~4.7uF
C2	0.22~0.47uf	0.47~1.0uf	0.47~1.0uf
R1	700 KΩ	1MΩ	1MΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	1.6MΩ	4MΩ	4MΩ
LCD SIZE	16x50mm	32x64mm	32x100mm
DOT CONFIGURATON	32x100	64x128	64x200

*1: As the input impedance of VR is high, a noise protection using short wire and cable shied is required.

*2: C1 and C2 depend on the capacity of the LCD panel to be driven. Seta value so that the LCD drive voltage may be stable.
[Setup example]
Turn on the voltage regulator and voltage follower and give an external voltage to VOUT. Display a horizontal-stripe LCD heavy load pattern and determine C2 so that the LCD drive voltage (V1 to V5) may be stable. However, the capacity value of C2 must be all equal. Next, turn on all the on-board power supplies and determine C1.

*3:LCD SIZE means the length and breadth of the display portion of the LCD panel.

Reset Circuit

When the RES input goes low, this LSI is initialized.

Initialized status
1.Display OFF
2.Normal display
3.ADC select: Normal display (ADC command D0=low)
4.Read modify write OFF
5.Power control register (D2, D1, D0)=(0,0,0)
6.Register data clear in serial interface
7.LCD power supply bias ratio 1/6(SED1530), 1/8(SED1531, SED1532)
8.static indicator: OFF
9.Display start line register set at line 1
10.Column address counter set at address 0
11. Page address register set at page 0
12.Output status register (D3)=(0)
13. Electronic control register set at 0
14.Test command OFF

As seen in Microprocessor Interface (Reference Example), connect The $\overline{RES}$ pin to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the SED1530 series does not use the internal LCD power Supply circuit, the $\overline{RES}$ must be low when the external LCD power Supply is turned on.

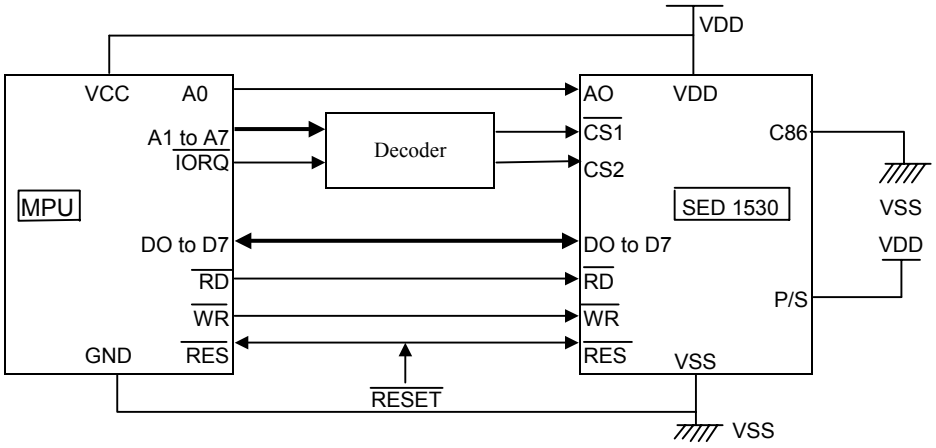
When $\overline{RES}$ goes low, each register is cleared and set to the above Initialized status. However, it has no effect on the oscillator circuit And output pins (FR, CL, DYO, D0 to D7).
The initialization by $\overline{RES}$ pin signal is always required during Power-on. If the control signal from the MPU is HZ, an over current May flow through the IC. A protection is required to prevent the HZ Signal at the input pin during power-on.

Be sure to initialize it by $\overline{RES}$ pin when turning on the power supply. When the reset command is used, only parameters 8 to 14 in the Above initialization are executed.

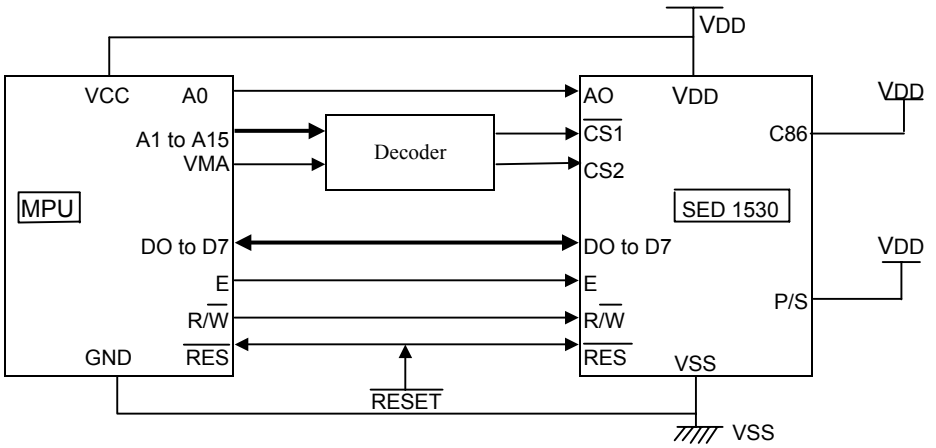
7.4. MICROPROCESSOR INTERFACE (Reference example)

The SED1530 series chips directly connect to 8080 and 6800-series microprocessors. Also serial interfacing requires less signal lines between them. When multiple chips are used in the SED 1530 series they can be connected to the microprocessor and one of them can be selected by Chip Select.

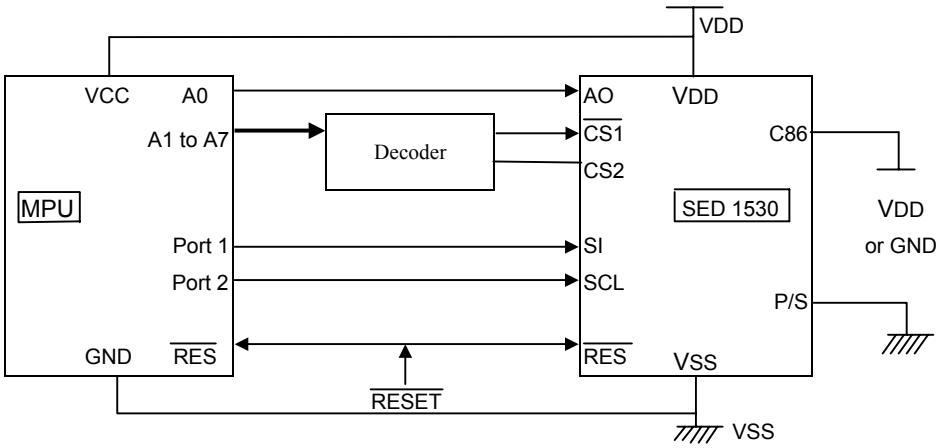
8080-series microprocessors



6800-series microprocessors



serial interface



7.5 FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The SED1530 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). When high or low is selected for the polarity of P/S pin,either8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, RAM data cannot be read out.

Table 1

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
H	Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
L	Serial input	$\overline{CS1}$	CS2	A0	-	-	-	SI	SCL	(HZ)

"-" must always be high or low.

Parallel input
When the SED1530 series selects parallel input(P/S= high),the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pin to go high or low as shown in Table2.

Table2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 to D7
H	6800 micro-processor bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
L	8080 micro-processor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	R/W	D0 to D7

Data Bus Signals

The SED1530 series identifies the data bus signal according to A0,E,R/W,($\overline{RD}$,$\overline{WR}$) signals.

Table3

Common	6800 processor	8080 processor		Function
A0	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (P/S is low)

The aerial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are rest.
Serial data of D7,D6,…,D0 is read at D7 in this sequence when serial clock (SCL) goes high. They are converted Into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.
The serial data input (SI) is determined to be the display data when A0 is high, and it is control data when A0 is low A0 is read on rising edge of every eighth clock signal.
Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

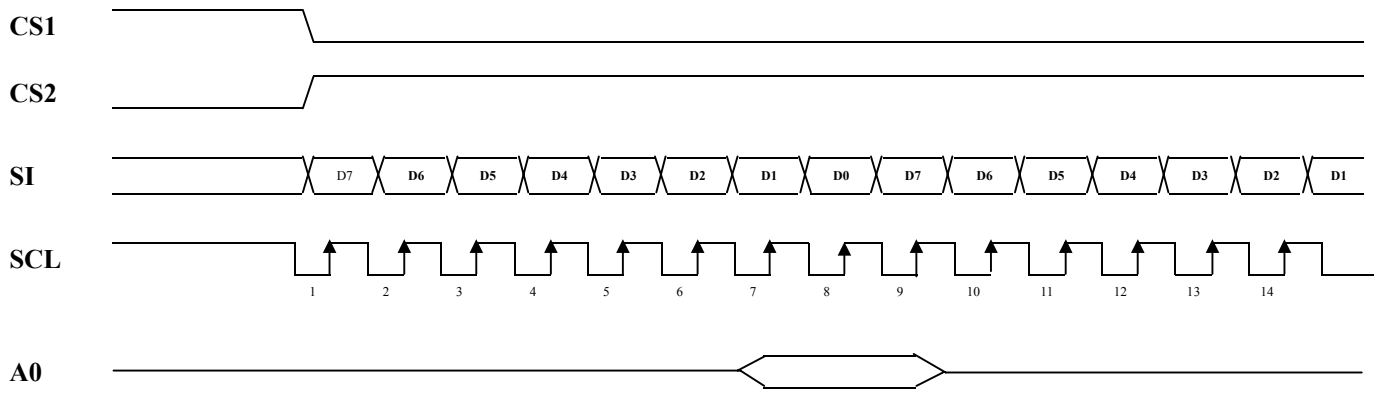


Figure 1

7.6. Column Address Counter

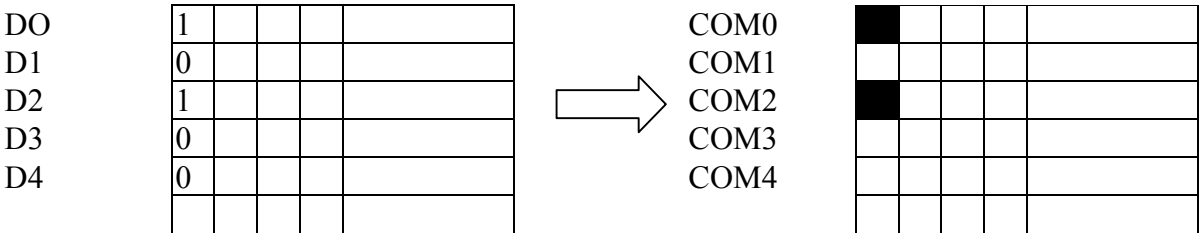
This is a 8bit presettable counter that provides column address to the display RAM(refer to Figure 4). It is incremented by 1 when a Read/write command is entered. However, the counter is not incremented but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register. When ADC Select command is issued to display inverse display, the Column address decoder inverts the relationship between RAM Column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another Page. Page address 8 (D3 is high, but D2, D1 and D0 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 65-column by 132-row(8-page by 8 bit+1) addressable array. Each pixel can be selected when page and column addresses are specified. The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple SED1530's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.



Display data RAM　　Display on LCD

7.7. Output Status Selector

The SED1530 series except SED1531 can set a COM output scan direction to reduce restrictions at LCD module assembly. This scan direction is set by setting "1"or "0" in the output status register D3.Fig.5 shows the status.

Fig.5 shows the status.

LCD output		O0			O131
ADC	"0"	0 (H)→			→83(H)
		Column address			
(D0)	"1"	83(H)←			←0(H)
		Display data RAM			
	D3				
SED1530D0*	0	SEG100		COM0----------COM31	
	1	SEG100		COM31----------COM0	
SED1530DA*	0	COM15-----0	SEG100		COM16----31
SED1530DF*	1	COM16----31	SEG100		COM15-----0

Relationship between display data RAM and addresses (if initial display line is 1CH):

Page address	Data		Line address	Common output
D3, D2 D1,D0 0,0,0,0	D0	Page0	00	COM 0
	D1		01	COM 1
	D2		02	COM 2
	D3		03	COM 3
	D4		04	COM 4
	D5		05	COM 5
	D6		06	COM 6
	D7		07	COM 7
0,0,0,1	D0	Page1	08	COM 8
	D1		09	COM 9
	D2		0A	COM10
	D3		0B	COM11
	D4		0C	COM12
	D5		0D	COM13
	D6		0E	COM14
	D7		0F	COM15
0,0,1,0	D0	Page2	10	COM16
	D1		11	COM17
	D2		12	COM18
	D3		13	COM19
	D4		14	COM20
	D5		15	COM21
	D6		16	COM22
	D7		17	COM23
0,0,1,1	D0	Page3	18	COM24
	D1		19	COM25
	D2		1A	COM26
	D3		1B	COM27
	D4		1C	COM28
	D5		1D	COM29
	D6		1E	COM30
	D7		1F	COM31
0,1,0,0	D0	Page4	20	COM32
	D1		21	COM33
	D2		22	COM34
	D3		23	COM35
	D4		24	COM36
	D5		25	COM37
	D6		26	COM38
	D7		27	COM39
0,1,0,1	D0	Page5	28	COM40
	D1		29	COM41
	D2		2A	COM42
	D3		2B	COM43
	D4		2C	COM44
	D5		2D	COM45
	D6		2E	COM46
	D7		2F	COM47
0,1,1,0	D0	Page6	30	COM48
	D1		31	COM49
	D2		32	COM50
	D3		33	COM51
	D4		34	COM52
	D5		35	COM53
	D6		36	COM54
	D7		37	COM55
0,1,1,1	D0	Page7	38	COM56
	D1		39	COM57
	D2		3A	COM58
	D3		3B	COM59
	D4		3C	COM60
	D5		3D	COM61
	D6		3E	COM62
	D7		3F	COM63
1,0,0,0	D0	Page8		COMS

1/64

Start

1/32

Column address	ADC															
	D0=0	00	01	02	03	04	05	06	07		80	81	82	83
	D0=1	83	82	81	80	7F	7E	7D	7C		03	02	01	00
	LCD OUT	O0	O1	O2	O3	O4	O5	O6	O7		O128	O129	O130	O131

Page 8 is accessed during 1/65 or 1/33 duty.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2)Initial Display Line	0	1	0	0	1	Start display address						Specifies RAM display line for COM0.
(3)Set page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register.
(4)Set column Address 4 higher bits	0	1	0	0	0	0	1	Higher Column address				Sets 4 high bits of column address of display RAM in register.
(4)Set column Address 4 higher bits	0	1	0	0	0	0	0	Lower Column address				Sets 4 lower bits of column address of display RAM in register.
(5)Read Status	0	0	1	Status				0	0	0	0	Reads the sets information.
(6)Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Read data from display RAM.
(8)ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9)Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high.
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display(0) or Entire Display ON (1).
(11)Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio.
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13)End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Output Status Register	0	1	0	1	1	0	0	0	*	*	*	Selects COM output scan direction. *Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode.
(17)Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets V5 output voltage to Electronic control register.
(18)Set Standby	0	1	0	1	0	1	0	1	1	0	0 1	Selects standby status. 0:OFF 1:ON
(19) Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(20)Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command Do not use!

Note: Do not use any other command, or the system malfunction may result.

8. QUALITY ASSURANCE

8.1 Test Condition

8.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 20 ± 5°C
Humidity : 65 ± 5%

8.1.2 Operation

Unless specified otherwise, test will be conducted with LCM in operation.

8.1.3 Container

Unless specified otherwise, vibration test will be conducted on module only.

8.1.4 Test Frequency

Single cycle.

8.1.5 Test Method

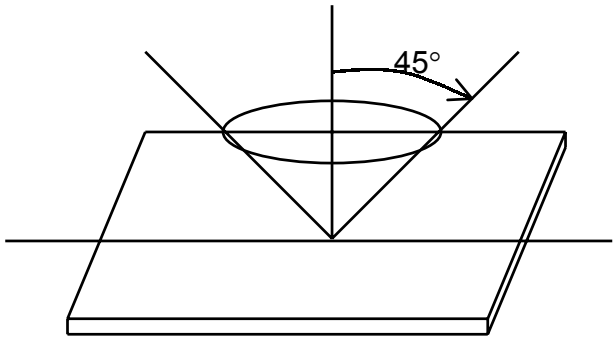
No.	Parameter	Conditions	Regulations
1	High Temperature Operating	50 ± 2 °C	Note 3
2	Low Temperature Operating	0 ± 2 °C	Note 3
3	High Temperature Storage	70 ± 2 °C	Note 3
4	Low Temperature Storage	-20 ± 2 °C	Note 3
5	Vibration Test (Non-operation state)	Total fixed amplitude : 1.5mm Vibration Frequency : 10 ~ 55Hz One cycle 60 seconds to 3 directions of X.Y.Z. for each 15 minutes	Note 3
6	Damp Proof Test (Non-operation state)	40°C ± 2°C, 90~95%RH, 96h	Note 1,2
7	Shock Test (Non-operation state)	To be measured after dropping from 60cm high once concrete surface in packing state	Note 3

Note 1: Returned under normal temperature and humidity for 4 hours.
Note 2: No dew condensation to be observed.
Note 3: No change on display and in operation under the test condition

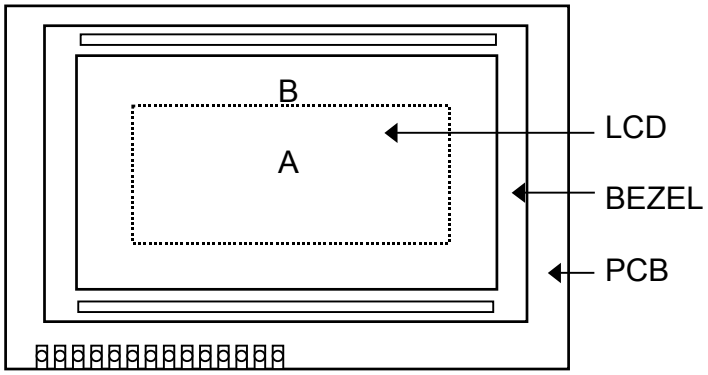
8.2 Inspection condition

8.2.1 Inspection conditions

The LCD shall be inspected under 40W white fluorescent light.

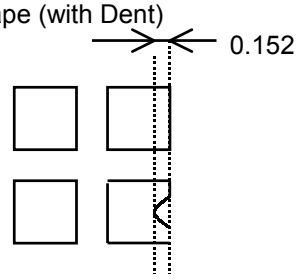


8.2.2 Definition of applicable Zones

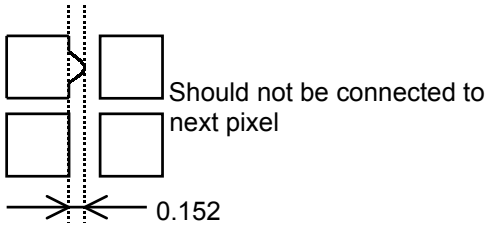


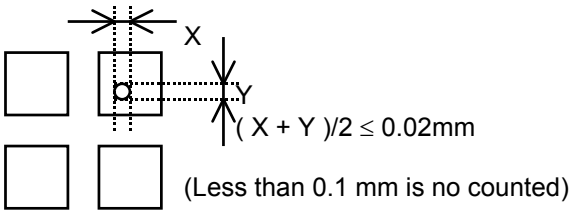
A : Display Area
B : Non-Display Area

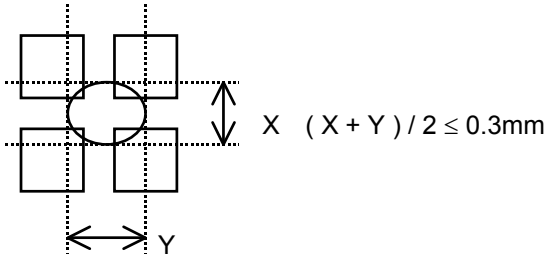
8.2.3 Inspection Parameters

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black or White spots</td><td>
<table>
<tr><th rowspan="2">Zone
Dimension</th><th colspan="2">Acceptable number</th><th rowspan="2">Class Of Defects</th><th rowspan="2">AQL Level</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>D < 0.15</td><td>*</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">2.5</td></tr>
<tr><td>0.15≤ D< 0.2</td><td>4</td><td>4</td></tr>
<tr><td>0.2 ≤ D ≤ 0.25</td><td>2</td><td>2</td></tr>
<tr><td>D ≤ 0.3</td><td>0</td><td>1</td></tr>
</table>
D = (Long + Short) / 2 * : Disregard
</td></tr>
<tr><td>2</td><td>Scratch, Substances</td><td>
<table>
<tr><th rowspan="2">Zone
X (mm) Y(mm)</th><th colspan="2">Acceptable number</th><th rowspan="2">Class Of Defects</th><th rowspan="2">AQL Level</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>*</td><td>0.04 ≥ W</td><td>*</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">2.5</td></tr>
<tr><td>3.0 ≥ L</td><td>0.06 ≥ W</td><td>4</td><td>4</td></tr>
<tr><td>2.0 ≥ L</td><td>0.08 ≥ W</td><td>2</td><td>3</td></tr>
<tr><td>—</td><td>0.1 < W</td><td>0</td><td>1</td></tr>
</table>
X : Length Y : Width * : Disregard
Total defects should not exceed 4/module
</td></tr>
<tr><td>3</td><td>Air Bubbles
(between glass & polarizer)</td><td>
<table>
<tr><th rowspan="2">Zone
Dimension</th><th colspan="2">Acceptable number</th><th rowspan="2">Class of Defects</th><th rowspan="2">AQL Level</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>D ≤ 0.15</td><td>*</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">2.5</td></tr>
<tr><td>0.15 < D ≤ 0.25</td><td>2</td><td>*</td></tr>
<tr><td>0.25 < D</td><td>0</td><td>1</td></tr>
</table>
* : Disregard
Total defects shall not excess 3/module.
</td></tr>
<tr><td>4</td><td>Uniformity of Pixel</td><td>(1) Pixel shape (with Dent)
 

</td></tr>
</table>

<table>
<tr><td>4</td><td colspan="2">Uniformity of Pixel</td><td>(2) Pixel shape (with Projection)
 

(3) Pin hole
 

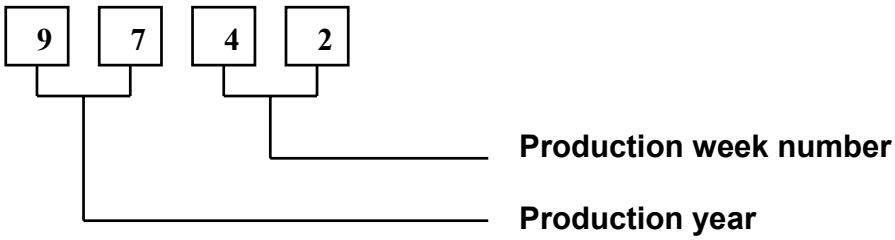
(4) Deformation
 

Total acceptable number : 1/pixel, 5/cell</td></tr>
<tr><td rowspan="3">Class of defects</td><td rowspan="2">Major</td><td>AQL 0.65%</td><td>Definition
It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.</td></tr>
<tr><td>AQL 1.00%</td><td>It is a defect that is likely to assembly size and not result in functioning problem.</td></tr>
<tr><td>Minor</td><td>AQL 2.5%</td><td>It is a defect that will not result in functioning problem with deviation classified.</td></tr>
</table>

8.3 Sampling Condition

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.
Lot size: Quantity of shipment lot per model.
Sampling type: normal inspection, single sampling
Inspection level: Level II
Sampling table: MIL-STD-105E

9. LOT NUMBERING SYSTEM



10. LCM NUMBERING SYSTEM

TG 963220 G R N N B – 01

VERSION :01

View direction & Temp. Range
A–Bottom view 6H & Normal temp.
B–Bottom view 6H & Wide temp.
C–Top View & Normal temp.
D–Top View & Wide temp.

Backlight Color
B –Blue
W –White
N –None

Backlight
S –edge light LED B/L
E –EL
N –No Back light

MODE
M – transmissive R – Reflective
F – transflective N - Negative

LCD type
G – STN Gray
S –STN Yellow
F – FSTN

Series code
963**20** –96 Dots X32 Dot, **2** LCD type, **0** PCB type

Model type
CM – Character Module
GM – Graphic Module
TG–Single TAB/COG Graphic Module
TX–Custom Single TAB/COG Graphic Module

11. PRECAUTION FOR USING LCM

1. LIQUID CRYSTAL DISPLAY (LCD)

LCD is made up of glass, organic sealant, organic fluid, and polymer based polarizers. The following precautions should be taken when handing,

(1). Keep the temperature within range of use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel off or bubble.

(2). Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

(3). Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

(4). Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

(5). Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.

(1). Do not tamper in any way with the tabs on the metal frame.

(2). Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.

(3). Do not touch the elastomer connector, especially insert an backlight panel (for example, EL).

(4). When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting . Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

(5). Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2. Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

(1). The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

(2). The modules should be kept in antistatic bags or other containers resistant to static for storage.

(3). Only properly grounded soldering irons should be used.

(4). If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.

(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

(6). Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

2.3 Soldering

(1). Solder only to the I/O terminals.

(2). Use only soldering irons with proper grounding and no leakage.

(3). Soldering temperature : 280°C ± 10°C

(4). Soldering time: 3 to 4 sec.

(5). Use eutectic solder with resin flux fill.

(6). If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed after wards.

2.4 Operation

(1). The viewing angle can be adjusted by varying the LCD driving voltage V0.

(2). Driving voltage should be kept within specified range; excess voltage shortens display life.

(3). Response time increases with decrease in temperature.

(4). Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear "fractured".

(5). Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

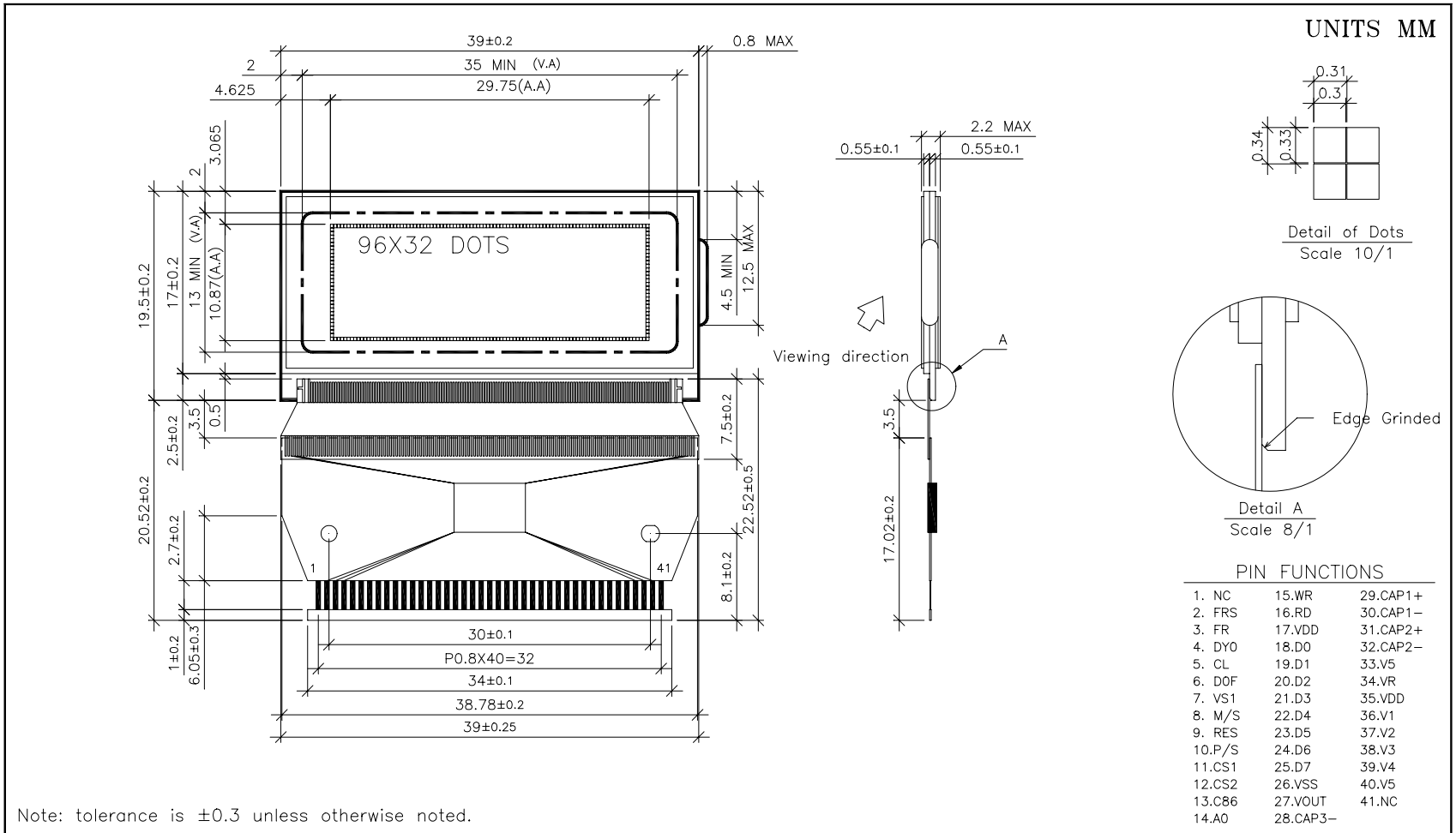
2.5 Storage

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

12 OUTLINE DRAWING



PIN FUNCTIONS

1. NC	15.WR	29.CAP1+
2. FRS	16.RD	30.CAP1−
3. FR	17.VDD	31.CAP2+
4. DY0	18.D0	32.CAP2−
5. CL	19.D1	33.V5
6. D0F	20.D2	34.VR
7. VS1	21.D3	35.VDD
8. M/S	22.D4	36.V1
9. RES	23.D5	37.V2
10.P/S	24.D6	38.V3
11.CS1	25.D7	39.V4
12.CS2	26.VSS	40.V5
13.C86	27.VOUT	41.NC
14.A0	28.CAP3−	

Note: tolerance is ±0.3 unless otherwise noted.

AUTH	DESCRIPTION	DATE	APPROVED

REVISIONS

ISSUE DATE:	08/08/02'
DRAWN:	
CHECK:	
APPROVE:	

DATA IMAGE Corporation

TITLE: LCM OUTLINE DIMENSION

A4 | DWG. NO. Q020811 | PART. NO. TG963220 | REV. 1

SCALE 2/1 | SHEET 1 OF 1

13. PACKAGE INFORMATION